receiver **410** that receives the signal to provide a sequence of symbols associated with the received signal in respective ones of a plurality of symbol positions. It is to be understood that the receiver **410** may be part of a transceiver, such as the transceiver **36** of **Figure 1** coupled to the antenna **48**. Thus, the system **400** may both receive and transmit the signals but, for the purposes of understanding the present invention, operations will be described with reference to receiving a signal in accordance with embodiments of the present invention.

Various circuits (or modules) of the illustrated embodiments of the present invention shown in **Figure 4** may be implemented, for example, by the processor **42** shown in **Figure 1** supported by use of the memory **38** also shown in **Figure 1**. An identification circuit **420** identifies a known block of the sequence of symbols. The known block contains known symbol values. Examples of such known blocks include the fields **210, 215** shown in **Figure 2** and the field **305** shown in **Figure 3**. The identification circuit **420** thereby further identifies an unknown block of the received sequence of symbols, where the unknown block contains unknown symbol values. As will be understood by those of skill in the art in light of this disclosure, the known symbol information may include pilot symbols or other known symbols at various locations in a received signal slot based on *a priori* information about the transmitted sequence of symbols, such as training information or known or predictable fields. As will be further described herein, the known symbols may also be generated by the receiving device using multi-pass demodulation where symbols are demodulated and error correction decoded and then reencoded and modulated.

The system **400** shown in **Figure 4** further includes a determination circuit **430** that determines a desired demodulation type for use in demodulating the unknown block (or blocks) based on the known symbol values. A detector circuit **440** detects an interferer signal characteristic discontinuity location in the unknown block. For example, such an interferer signal characteristic discontinuity may comprise an interferer signal slot misalignment relative to a slot alignment of a desired signal component of the received signal as shown by the respective timing of the desired (D) interferer (I) signals shown in **Figures 2** and **3**.

The system **400** further includes a demodulator circuit **450** that demodulates the unknown fields to provide symbol estimates for the received signal to the receiving system **400**. The demodulator **450** demodulates the unknown block symbols

using a first selected demodulation type between the interferer signal characteristic discontinuity and a known block and a second selected demodulation type on another portion of the unknown block. The first selected modulation type and the second selected modulation type in the illustrated embodiments are selected based on the determined desired modulation type for use in demodulating the unknown block (or blocks) and the detected interferer signal characteristic discontinuity location. Such operations are illustrated, for example, with respect to a single and two known fields by the selection of conventional demodulation (CD) or joint demodulation (JD) and respective directions for such demodulation (where bi-directional demodulation is desired) in **Figures 2** and **3**.

Operations for further embodiments of the present invention utilizing multi-pass demodulation will now be described with reference to the schematic block diagram illustration of **Figure 5**. It is to be understood that the demodulator **450** may be a multi-pass demodulator and that aspects of multi-pass demodulation may be utilized with the embodiments described in reference to **Figure 4** as well as to those in reference to **Figure 5**. It will further be understood from the description which follows that an environment including slot misaligned interferer signals may be addressed by the slot partition approach which will be described herein with reference to **Figure 5** and various of the flowcharts, either alone or in combination with the selection of a type and direction of demodulation within an unknown field based on a detected interferer discontinuity location as described previously.

As shown in **Figure 5**, the system **500** for processing a received signal in the illustrated embodiments includes a receiver **510** that receives the signal to provide a sequence of symbols associated with the received signal in respective ones of a plurality of symbol positions. As with the receiver **410** of **Figure 4**, the receiver **510** may be a transceiver, such as the transceiver **36** coupled to the antenna **48** as illustrated in **Figure 1**. A multi-pass demodulator **550** is provided which includes a first pass demodulator/decoder that first pass demodulates and decodes the sequence of symbols to provide error corrected decoded bits. The demodulator **550** further operates as a second pass demodulator that demodulates subfields of the received symbols using determined desired demodulation types as will be further described herein. While shown as implemented in a single demodulator **550**, it is to be

understood that the first pass demodulator and second pass demodulator may be separate circuits or modules.

A reencoder circuit **560** re-encodes and modulates the error corrected decoded bits from the first pass module of the demodulator **550** to provide a second sequence of symbols associated with the received signal in respective ones of the plurality of symbol positions. The second sequence of symbols includes known symbol values based on the first pass demodulating and decoding operations. Such operations are further illustrated in **Figure 9** at blocks **900-915** and in **Figure 10** blocks **1000** and **1015** as will be described further herein.

The partition circuit **570** partitions the sequence of symbols received by the receiver **510** into a plurality of subfields. Ones of the subfields include a plurality of the known symbol values with a sufficient number of known symbol values included in the subfields so as to determine a desired modulation type for use in demodulating the subfields based on the included plurality of known symbol values. A determination circuit **530** determines the desired demodulation type for use in demodulating the subfields based on the known symbol values of the respective ones of the subfields from the partition circuit **570**. Also shown in **Figure 5**, is an optional detector circuit **540** that detects an interferer signal characteristic discontinuity location in the sequence of symbols, which detected location, may be used, for example, in selecting the transition points between respective subfields.

The functionality of a receiver for the embodiments illustrated in **Figures 1-5** may be implemented using discrete hardware components, a single application specific integrated circuit (ASIC), a programmed digital signal processor or microcontroller or combinations thereof referred to generally herein as a circuit or module. Moreover, **Figures 1-5** illustrate exemplary architectures that may be used for processing a received signal in accordance with embodiments of the present invention. It will be understood that the present invention is not limited to these configurations, but is intended to encompass any configuration capable of carrying out the operations described herein regardless of how the functionality is grouped across different circuit devices or modules.

The present invention is described hereinafter with reference to flowchart and/or block diagram illustrations of methods, apparatus, and computer program products in accordance with exemplary embodiments of the invention. It will be